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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/103,873 06/24/98 NAGANO

Y YAO-3950

MMC2/0130

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EXAMINER

DIAZ, J

ART UNIT

PAPER NUMBER

2815

DATE MAILED:

01/30/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/103,873

Applicant(s)

NAGANO ET AL.

Examiner

José R. Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☒ The proposed drawing correction filed on 09 November 2000 is: a) ☒ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

DETAILED ACTION

Drawings

➤ The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on November 9, 2000 have been approved.

Claim Rejections - 35 USC § 102

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

➤ Claims 1-2 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Applicant's Specification.

Regarding claim 1, Applicant acknowledges that is well known in the art to form a semiconductor device comprised of: an integrated circuit (4) on a supporting substrate (1); a capacitor (10) having a lower electrode (7), a dielectric film (8), and an upper electrode (9); a first interlayer insulating film (11) provided so as to cover the capacitor; a first interconnect (14) electrically connected to the integrated circuit (4) and the capacitor (10) through a first contact hole (12) formed in the first interlayer insulating film (11); a second interlayer insulating film (15) provided so as to cover the first interconnect (14); a second interconnect (15) electrically connected to the first interconnect (14) through a second contact hole (12) formed in the second interlayer insulating film (15); and a passivation layer (18) provided so as to cover the second interconnect (15) (See figures 10A-10E).

Regarding claim 2, Applicant acknowledges that the dielectric film (8) is formed either a dielectric material having a high dielectric constant or ferroelectric material (Page 2, lines 26-28).

The claim(s) contain method of making characteristics given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. In the instance case, Applicant claims an ozone-TEOS process to form the second interlayer insulating film which is a well known process used in the art to form a silicon dioxide layer to cover a capacitor (See for example: Patel et al., EU Patent No. 0557937, col. 7 lines 5-10).

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102((e), f) or (g) prior art under 35 U.S.C. 103(a).

➤ Claims 3-4, 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Yoshizumi et al. (US Patent No. 5,444,012).

Applicant's Specification, as stated supra, essentially discloses the claimed invention but fails to show a second interconnect on the second interlayer insulating film provided so as to cover at least a part of the capacitor. Regarding claim 3, Yoshizumi et al. teach that it is well known in the art to form a second interconnect (DL₁, DL₂) on selective portions of an insulating film (35) so as to cover at least a part of the capacitors (C₁, C₂) (Figure 24). Yoshizumi et al. provide motivation to use such a layer in that it provides a connection to the first interconnect (33) (column 21, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include providing a second interconnect on the second interlayer insulating film so as to cover

at least a part of the capacitor as taught by Yoshizumi et al. since such modification would result in a connection between the first and second interconnect, as described in column 21, lines 13-15 of Yoshizumi et al.

Moreover, Applicant's Specification fails to show a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film. Regarding claim 4, Yoshizumi et al. teach that it is well known in the art to form a passivation layer from a laminate including a silicon oxide film (37a, 37b) and a silicon nitride film (37c) (Figure 28). Yoshizumi et al. provide motivation to use such a layer in that there is no increase in the number of photomasks and the number of steps in etching (column 23, lines 57-61). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include providing a passivation layer from a laminate including a silicon oxide film and a silicon nitride film as taught by Yoshizumi et al. since such modification would result in a decrease of the number of photomasks and the number of steps in, as described in column 23, lines 57-61 of Yoshizumi et al.

Furthermore, Applicant's Specification fails to teach that the first and second interconnect layers are formed from a laminate including aluminum and titanium tungsten. Regarding claims 6 and 10, Yoshizumi et al. teach that it is well known in the art to use a three-layer film formed by successive lamination of TiW film, aluminum alloy film, and TiW as the wiring material (column 20, lines 54-56). Yoshizumi et al. provide motivation to use such material in that the wiring line can be prevented from being broken by electromigration (column 21, lines 5-7). Therefore, it would have been

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obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include a laminate of TiW film, aluminum alloy film, and TiW as the wiring material as taught by Yoshizumi et al. since such modification would result in a wiring line having no cracks, as described in column 21, lines 5-7 of Yoshizumi et al.

➤ Claims 5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Matsuura et al. (US Patent No. 5,132,774).

Applicant's Specification, as stated supra, essentially discloses the claimed invention but fails to show a hydrogen supplying layer. Regarding claim 5, Matsuura et al. teach forming a hydrogen supplying layer (i.e. nitride layer) (13) (See Figure 5B). Matsuura et al. provide motivation to use such a layer in that the stress of the interlayer insulating film (14) is relaxed (column 7, lines 3-6 and 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant to include a hydrogen supplying layer as taught by Matsuura et al. since such modification would result in a interlayer insulating film having no stress, as described in column 7, lines 3-6 and 7-10 of Matsuura et al.

Furthermore, Applicant's Specification fails to teach a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less, a tensile stress of $1 \times 10^7\text{ dyn/cm}^2$ to $3 \times 10^9\text{ dyn/cm}^2$, and a thickness of $0.3\text{ }\mu\text{m}$ to $1\text{ }\mu\text{m}$. Regarding claim 7, Matsuura et al. teach a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} (Figure 3B).

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Regarding claim 9, Matsuura et al. teach that it is known in the art to provide an interlayer insulating film (4) having a thickness of about 5 μm (column 1, lines 30-35). Regarding claim 8, the interlayer insulating film (14) disclosed by Matsuura et al. has the same properties that Applicant intends to claim, hence it is inherent that the second interlayer insulating film of the semiconductor device disclosed by Matsuura et al. has a tensile stress of $1 \times 10^7 \text{ dyn/cm}^2$ to $3 \times 10^9 \text{ dyn/cm}^2$. Matsuura et al. provide motivation to use such a layer having a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} , a thickness of about 5 μm , and a tensile stress of $1 \times 10^7 \text{ dyn/cm}^2$ to $3 \times 10^9 \text{ dyn/cm}^2$ in that the insulation of the semiconductor device is improved by feature of an interlayer insulating film (column 3, lines 23-25). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include a layer having a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} , a thickness of about 5 μm , and a tensile stress of $1 \times 10^7 \text{ dyn/cm}^2$ to $3 \times 10^9 \text{ dyn/cm}^2$ as taught by Matsuura et al. since such modification would result in an interlayer insulating film having no cracks, as described in column 3, lines 23-25 of Matsuura et al.

Response to Arguments

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.


Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
January 29, 2001


EDDIE C. LEE
PRIMARY EXAMINER